AD8310 Evaluation Board

EVAL-AD8310EB

BOARD DESCRIPTION

The AD8310 evaluation board has been carefully laid out and tested to demonstrate the specified high speed performance of the device. Figure 1 shows the schematic of the evaluation board. Connectors INHI, INLO, and VOUT are SMA type; supply and ground are connected to vector pins TP1 and TP2, switches and component settings for different setups are described in Table I. The layout and silkscreen for the component side of the board are shown in Figures 2 and 3. For ordering information, please refer to the Ordering Guide.

ORDERING GUIDE

Model	Package Description
AD8310-EVAL	Evaluation Board

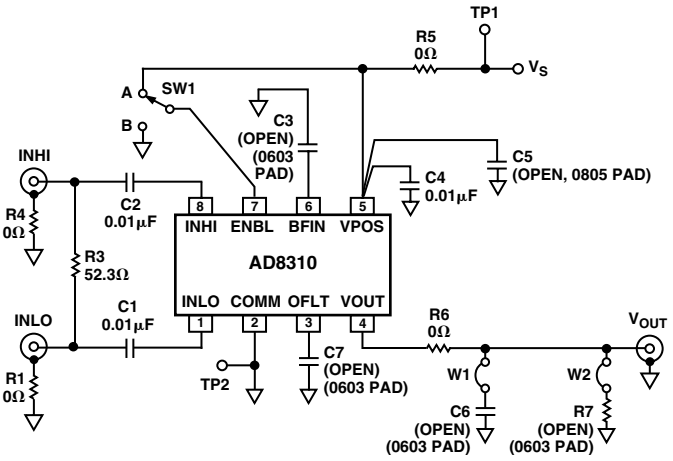

Figure 1. Evaluation Board Schematic

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8310EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

REV. 0

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Table I. Evaluation Board Setup Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins	Not Applicable
SW1	Device Enable. When in Position A, the ENBL pin is connected to $+V_S$ and the AD8310 is in normal operating mode. In Position B, the ENBL pin is connected to ground putting the device in sleep mode.	SW1 = A
R1/R4	SMA Connector Grounds. Connects common of INHI and INLO SMA connectors to ground. Can be used to isolate the generator ground from the evaluation board ground (see Figure 26 of the AD8310 data sheet).	R1 = R4 = 0 Ω
C1, C2, R3	Input Interface. R3 (52.3 Ω) combines with the AD8310's 1 kΩ input impedance to give an overall broadband input impedance of 50 Ω. C1, C2, and the AD8310's input impedance combine to set a high-pass input corner of 32 kHz. Alternatively, R3, C1, and C2 can be replaced by an inductor and matching capacitors to form an input matching network. See Input Matching section of the AD8310 data sheet for more detail.	R3 = 52.3 Ω C1 = C2 = 0.01 μF
C3	RSSI (Video) Bandwidth Adjust. The addition of C3 (Farads) will lower the RSSI bandwidth of the VLOG output according to the equation: $C_{FILT} = 1/(2\pi \times 3\ k\Omega \times \text{Video Bandwidth}) - 2.1\ pF$.	C3 = Open
C4, C5, R5	Supply Decoupling. The nominal supply decoupling of 0.01 μF (C4) can be augmented by a larger capacitor in C5. An inductor or small resistor can be placed in R5 for additional decoupling.	C4 = 0.01 μF C5 = Open, R5 = 0 Ω
R6	Output Source Impedance. In cable-driving applications, a resistor (typically 50 Ω or 75 Ω) can be placed in R6 to give the circuit a back-terminated output impedance.	R6 = 0 Ω
W1, W2, C6, R7	Output Loading. Resistors and capacitors can be placed in C6 and R7 to load test V_{OUT}. Jumpers W1 and W2 are used to connect/disconnect the loads.	C6 = R7 = Open W1 = W2 = Installed
C7	Offset Compensation Loop. A capacitor in C7 will reduce the corner frequency of the offset control loop in low frequency applications.	C7 = Open

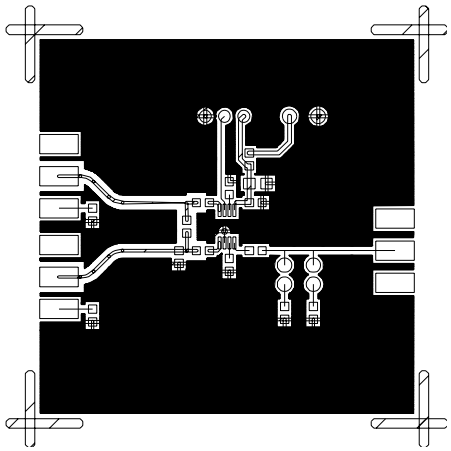

Figure 2. Layout of Component Side of Evaluation Board

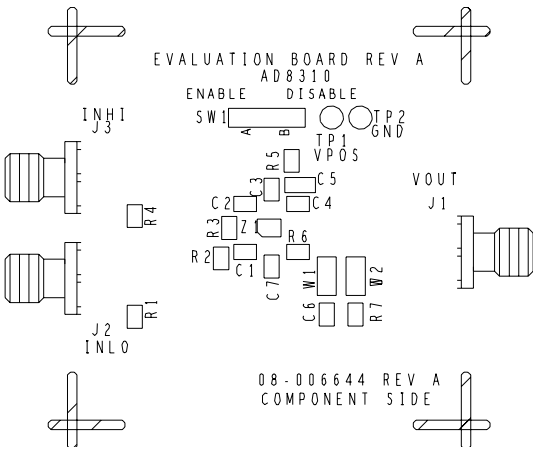

Figure 3. Component Side Silkscreen of Evaluation Board